Remarks:

Reconsideration of the application is requested.

Claims 1-14 are now in the application. Claims 11-14 have been amended and claims 15-17 have been cancelled.

In item 6 on page 4 of the above-identified Office action, the specification has been objected to because of informalities.

The indication of the informalities is appreciated and they have been corrected.

In item 7 on page 4 of the above-identified Office action, claims 11, 13, and 14 have been objected to because of informalities.

Applicant appreciates the suggested changes that have been offered by the Examiner and the claims have been amended in accordance with those suggestions.

In item 9 on page 5 of the above-identified Office action, claims 11 and 13 have been rejected under 35 U.S.C. § 112, first paragraph.

Copies from chapters relating to change pumps and PLL's in two textbooks have been provided with this response. The two

textbooks are: "Design Of Analog CMOS Integrated Circuits", and "The Design of CMOS Radio Frequency Integrated Circuits". It is believed that reference to this material may be helpful with regard to understanding the term, "a charge pump for integrating ..." in claim 11. Relevant portions have been underlined and/or highlighted.

The term, "integration polarity" has been deleted from the claims.

Claims 11 and 13 have been amended to specify that the phase regulation direction is changed. Support for the changes can be found by referring to Figs. 1, 8, and 10, for example. Additional support can be found by referring to pages 9-13 of the application.

In item 10 on page 6 of the above-identified Office action, claim 14 has been rejected under 35 U.S.C. § 112, first paragraph.

Claim 14 has been changed to specify that the change is based on the input signal. Support for the changes can be found by referring to Figs. 1, 8, and 10 and to pages 9-13 of the application.

In item 12 on page 7 of the above-identified Office action, claims 11-17 have been rejected as being indefinite under 35 U.S.C. § 112, second paragraph.

The terms, "integration polarity" and "controller" have been deleted from the claims. The term regulation signal is now used. With regard to the hysteresis, the claim language has been changed to specify that the change in the regulation direction has a hysteresis behavior. Support for the changes can be found by referring to Figs. 1, 8, and 10, for example. Additional support can be found by referring to pages 9-13 of the application.

The hysteresis is caused by the slight overlapping of the phase regions Q1, Q2, Q3, and Q4 in order to avoid a switching back and forth of the phase regulation direction in phase positions of exactly 135, 225, 315, or 45 degrees.

It is accordingly believed that the specification and the claims meet the requirements of 35 U.S.C. § 112, first and second paragraphs. Should the Examiner find any further objectionable items, counsel would appreciate a telephone call during which the matter may be resolved. The above noted changes to the claims are provided solely for the purpose of satisfying the requirements of 35 U.S.C. § 112. The changes are neither provided for overcoming the prior art nor do they

narrow the scope of the claims for any reason related to the statutory requirements for a patent.

It is believed to be clear that none of the references, whether taken alone or in any combination, either show or suggest the features of claims 11, 13, or 14. Claims 11, 13, and 14 are, therefore, believed to be patentable over the art and since all of the dependent claims are ultimately dependent on claim 11, they are believed to be patentable as well.

In view of the foregoing, reconsideration and allowance of claims 11-14 are solicited.

In the event the Examiner should still find any of the claims to be unpatentable, he is respectfully requested to telephone counsel so that, if possible, patentable language can be worked out.

Petition for extension is herewith made. The extension fee for response within a period of one-month pursuant to Section 1.136(a) in the amount of $110.00 in accordance with Section 1.17 is enclosed herewith.

Please charge any other fees which might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

Respectfully submitted,

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June 13, 2003

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M&N-IT255

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Karl Schrödinger

Applic. No. : 09/992,281

Filed : November 16, 2001

Title : Method and Apparatus for Producing a Clock Output Signal

Examiner : Linh M. Nguyen

Group Art Unit : 2816

VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Specification:

On page 9, line 20 through page 10:

Figs. 3 and 4 show the circuit contained in the phase shifter 2 from [Fig. 1] Fig 2. Fig. 3 shows a circuit for producing the clock signal C_{out} by mixing the clock signals C0 to C3. These four clock signals C0 to C3 are shown in Fig. 5. The circuit contains two mixers, which are respectively operated with the appropriate clock phases and operate differentially on the same load resistors R1 and R2. A capacitor C1 (optional) is used for band-limiting, since only the fundamentals of the individual phases of the clock signals C1 to C3 need to be mixed (added), and harmonics need to be filtered out accordingly. The control voltages U0 to [U4] U4

are used to weight the respective clock signals C0 to C3 in an appropriate manner.

In the Claims:

Claim 11 (amended). A control loop, comprising:

a phase shifter for producing an output with a first clock phase;

a phase detector for detecting a phase difference between a second clock phase of a data signal and the first clock phase, said phase detector producing an output signal based on the detected phase difference;

a charge pump for integrating the output signal of said phase detector, said charge pump [having an integration polarity] producing a regulation signal for said phase shifter; and

said phase shifter changing over a phase regulation direction at predetermined switching points based on said regulation signal;

said changing over of said phase regulation direction being performed with a hysteresis behavior

[a controller for changing over the integration polarity of said charge pump at predetermined switching points based on the detected phase difference;

the switching points being subject to hysteresis].

Claim 12 (amended). The control loop according to claim 11, in combination with a delay locked loop circuit, said delay locked loop circuit having a delay locked loop control loop including said phase shifter, said phase detector, and said charge pump[, and said controller].

Claim 13 (amended). A method for producing a clock signal, which comprises:

detecting a phase difference between a clock phase of a first input signal [for a phase shifter] and a clock phase of a first output signal of the phase shifter;

producing a second output signal based on the detected phase difference;

producing a second input signal for the phase shifter by integrating the second output signal; and

[changing over a polarity of the integrating at predetermined switching points based on the detected phase difference, the switching points being subject to hysteresis]

changing a phase regulation direction of the phase shifter at predetermined switching points based on the second input signal, the changing over of the phase regulation direction being performed with a hysteresis behavior.

Claim 14 (amended). A [charge pump] phase shifter for producing an output signal, which comprises:

a [charge pump] circuit for receiving an input signal having a phase;

said [charge pump] circuit also for producing an output signal having a phase;

the output signal selected from the group consisting of a proportional signal essentially proportional to the phase of the input signal and an inversely proportional signal essentially inversely proportional to the phase of the input signal;

said [charge pump] circuit being designed such that the output signal changes [from] between the proportional signal and the

inversely proportional signal at predetermined switching points [at which a predetermined jump in the phase of the output signal takes place] based on the input signal of said charge pump.